REMARKS

Reconsideration of this application as amended is respectfully requested.

Claim 1 stands rejected under 35 U.S.C. § 102(b) as being unpatentable over U.S. Pat. No. 5,361,373 of Gilson ("Gilson").

Claims 1-3 stand rejected under 35 U.S.C. § 102(b) as being unpatentable over U.S. Pat. No. 5,668,815 of Gittinger et al. ("Gittinger").

The specification has been amended at page 14, line 25; and page 19, line 2 to add U.S patent application numbers and to remove references to incorporation by reference.

It is submitted that the amendments to the specification do not add new matter.

Claim 1 has been amended. Claims 2-3 have been canceled. New claims 14-20 have been added.

Support for claims 1 and 14-20 is found in the specification at pages 8, 12, 16-18, and 21, and Figures 1-3C.

It is respectfully submitted that in view of the above-listed support, claims 1 and 14-20 do not add new matter.

It is respectfully submitted that amended claim 1 and new claims 14-20 are within the subject matter of the group elected with respect to the restriction requirement.

The Examiner has rejected claim 1 under 35 U.S.C. § 102(b) as being anticipated by Gilson. The Examiner has stated that

> Gilson teaches a Field Programmable Gate Array (FPGA) 12 including a computing device 10 ("configurable system on a chip"). The computing device 10 includes a configuration memory array 20 ("configurable system logic"). A "system bus" is represented by the bus interconnecting the host I/F, configuration memory array and reconfigurable instruction execution unit. Configuration data is loaded into the configuration memory array 20 over the bus by Host 40 ("configuring a memory cell in the CSL using the system bus"). See column 5, lines 46-50. The configuration data is then utilized to configure the

> reconfigurable instruction execution unit ("reading the memory cell in the CSL using the system data bus"). See column 7, lines 26-35.

(p.3 Office Action 18-May-01).

Applicants respectfully submit that amended claim 1 is not anticipated under 35 U.S.C. § 102(b) by Gilson. Amended claim 1 includes the limitation

> determining if the system bus is controlled for configuration by a first device selected from a group consisting of on-chip central processing unit (CPU), direct memory access (DMA) controller, and external control device.

(Amended Claim 1).

Gilson discloses an integrated circuit computing device wherein

> Host 40 reconfigures the FPGA 12 which causes new configuration data to be written into the Configuration Memory Array 20. Now referring to FIG. 2, the effect of this new configuration data is to . . . change the programming of the Logic Blocks 34 that comprise the Reconfigurable Instruction Execution Unit 16 such that the desired complex operation can be accomplished by the newly configured hardware on data that already exists within the Reconfigurable Instruction Execution Unit 16.

(Gilson Col. 7, lines 22-35).

Although Gilson discloses that host 40 reconfigures the FPGA 12 (col. 7 line 22), Gilson fails to disclose determining if the system bus is controlled for configuration by a first device selected from a group consisting of on-chip central processing unit (CPU), direct memory access (DMA) controller, and external control device. In fact, Gilson fails to disclose that FPGA 12 has a DMA controller with which to control the system bus for configuration.

It is therefore respectfully submitted that the method of amended claim 1 that includes determining if the system bus is controlled for configuration by a first device selected from a group consisting of on-chip central processing unit (CPU), direct memory access (DMA) controller, and external control device is not anticipated by Gilson.

The Examiner has rejected claims 1-3 under 35 U.S.C. § 102(b) as being anticipated by Gittinger. The Examiner has stated that

> Gittinger et al. teaches a microcontroller formed on a single monolithic semiconductor substrate ("configurable system on a chip"). The microcontroller includes a processor core 16 ("CPU"), DMA control 20, a central bus 34 ("system bus") and internal memory 30 ("configurable system logic"). See figure 1. The internal memory 30 is initialized ("configuring a memory cell in the CSL using the system bus") with a selected background pattern. See column 12, lines 40-42. Then the background pattern is read from the memory ("reading the memory cell in the CSL using the system bus"). See column 13, lines 21-23.

(pp. 3-4 Office Action 18-May-01)

Applicants respectfully submit, however, that amended claim 1 is not anticipated under 35 U.S.C. § 102(b) by Gittinger. Amended claim 1 includes the limitation

> determining if the system bus is controlled for configuration by a first device selected from a group consisting of on-chip central processing unit (CPU), direct memory access (DMA) controller, and external control device

(Amended Claim 1).

The microcontroller in Gittinger fails to discloses "determining if the system bus is controlled for configuration by a . . . external control device" (claim 1). Gittinger fails to disclose a method of controlling internal busing 34 of microcontroller 10 with an external device. Without disclosing a method for determining if the system bus is controlled for configuration by an external control device, Gittinger fails to disclose the method of amended claim 1.

Furthermore, Gittinger is not a configurable system on a chip. In contrast, Gittinger discloses that a

> Microcontroller 10 includes a clock/power management unit 12, an interrupt control unit 14, a processor core 16, a timer control unit 18, a DMA control unit 20, a programmable input/output (PIO) unit 22, an asynchronous serial interface 24, a synchronous serial interface 26, a chip select unit 28, an internal memory 30, and a bus interface unit 32.

(Gittinger Col. 5, lines 19-26) (emphasis added).

The microcontroller of Gittinger does not include configurable system logic ("CSL"). Applicants respectfully submit that the internal memory 30 of Gittinger is not CSL thus Gittinger fails to disclose the following limitations of amended claim 1.:

> configuring a memory cell in the CSL using the system bus; and
> reading the memory cell in the CSL using the system bus

(Amended Claim 1).

Given that new claims 14-20 depend from claim 1, applicants also submit that new claims 14-20 are not anticipated or rendered obvious in view of the references cited by the Examiner.

It is respectfully submitted that in view of the remarks set forth herein, the above rejections have been overcome.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment.

Please charge any fees not covered by any checks submitted herewith to our Deposit Account No. 02-2666.

Respectfully submitted,
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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Please amend the paragraph beginning on page 14, line 21 in the following manner:

CPU 206 also controls the selective enabling of PIOs 201A in step 325, thereby providing certain output signals before other output signals from CSoC 101. A more detailed description of PIOs 201A is provided in U.S. Patent Application [Serial] No. 09/418,416 [_____ (TRI-004)], filed on October 15, 1999 by Triscend Corporation, and entitled "An Input/Output Circuit With User Programmable Functions [, which is incorporated by reference herein]."

Please amend the paragraph beginning on page 18, line 31 in the following manner:

Determining the states of the configuration memory cells in logic block tiles 501 is highly advantageous in debug operations. For a more detailed description of such debug operations, see U.S. Patent Application [Serial] No. 09/418,948 [_____ (TRI-002)], entitled "Bus Mastering Debugging System For Integrated Circuits", filed by Triscend Corporation on October 15, 1999[, and incorporated by reference herein].

IN THE CLAIMS

Please cancel claims 2-3 without prejudice.

Please amend claim 1 as follows:

1. (Amended) A method of using a system bus on a configurable system on a chip (CSoC), the CSoC including configurable system logic (CSL), the method comprising:

determining if the system bus is controlled for configuration by a first device selected from a group consisting of on-chip central processing unit (CPU), direct memory access (DMA) controller, and external control device;

configuring a memory cell in the CSL using the system bus; and

reading the memory cell in the CSL using the system bus.